

Fig 1

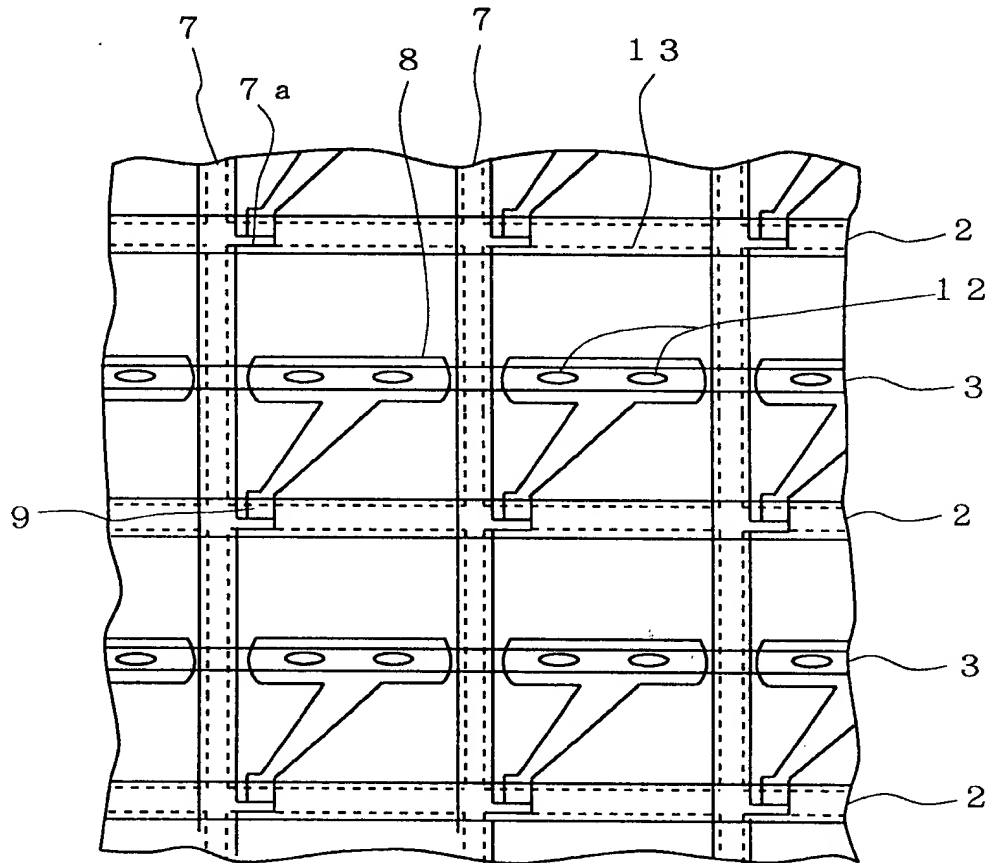
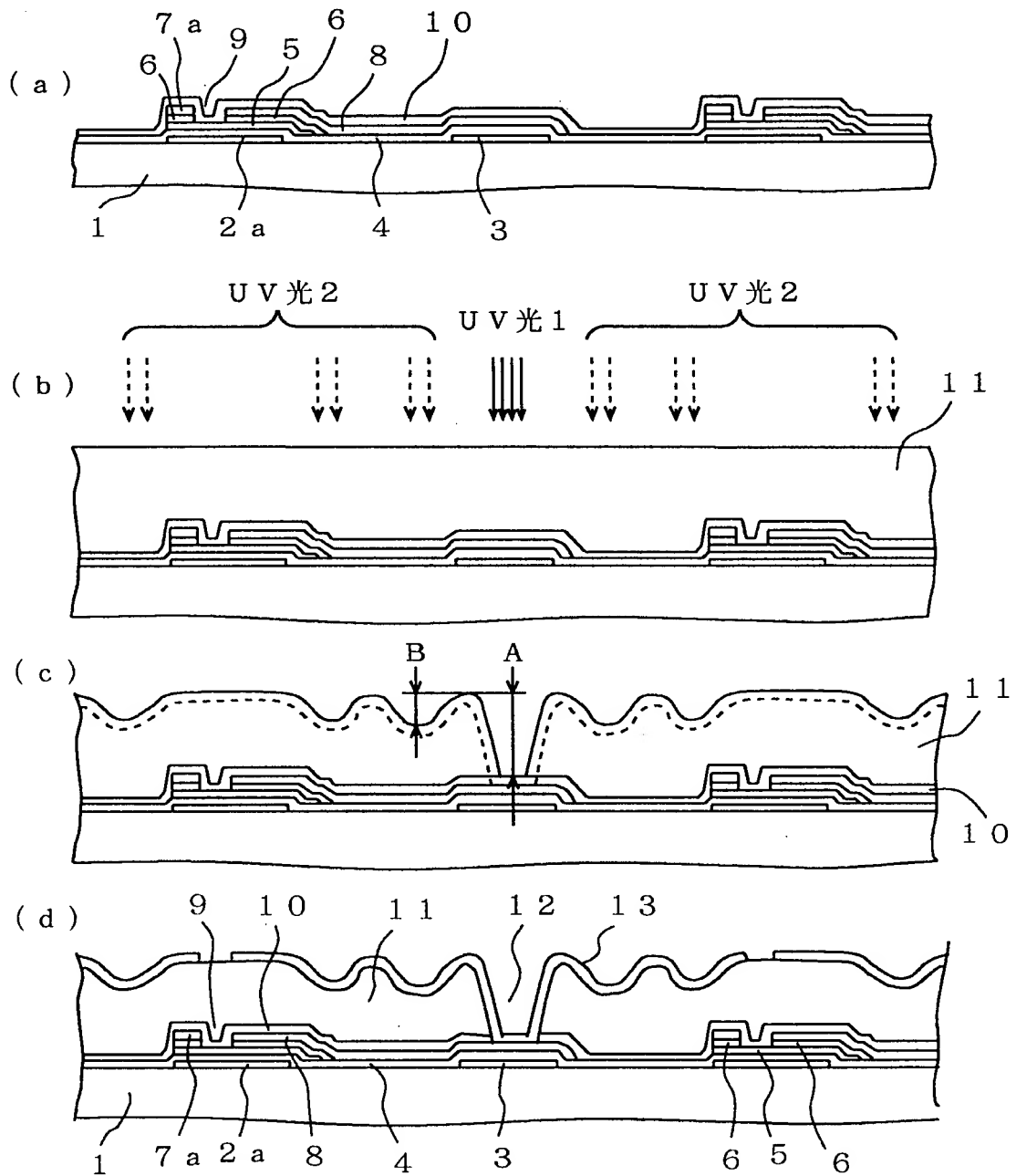


Fig 2



- | | | |
|----------------|----------------------|---------------|
| 1 : 絶縁性基板 | 6 : $n^+ - a - Si$ 膜 | 11 : 層間絶縁膜 |
| 2 : ゲート電極配線 | 7 : ソース電極配線 | 12 : コンタクトホール |
| 2a : ゲート電極 | 7a : ソース電極 | 13 : 反射画素電極 |
| 3 : 共通電極配線 | 8 : ドレイン電極 | |
| 4 : ゲート絶縁膜 | 9 : チャンネル部 | |
| 5 : $a - Si$ 膜 | 10 : パッシベーション膜 | |

Fig 3

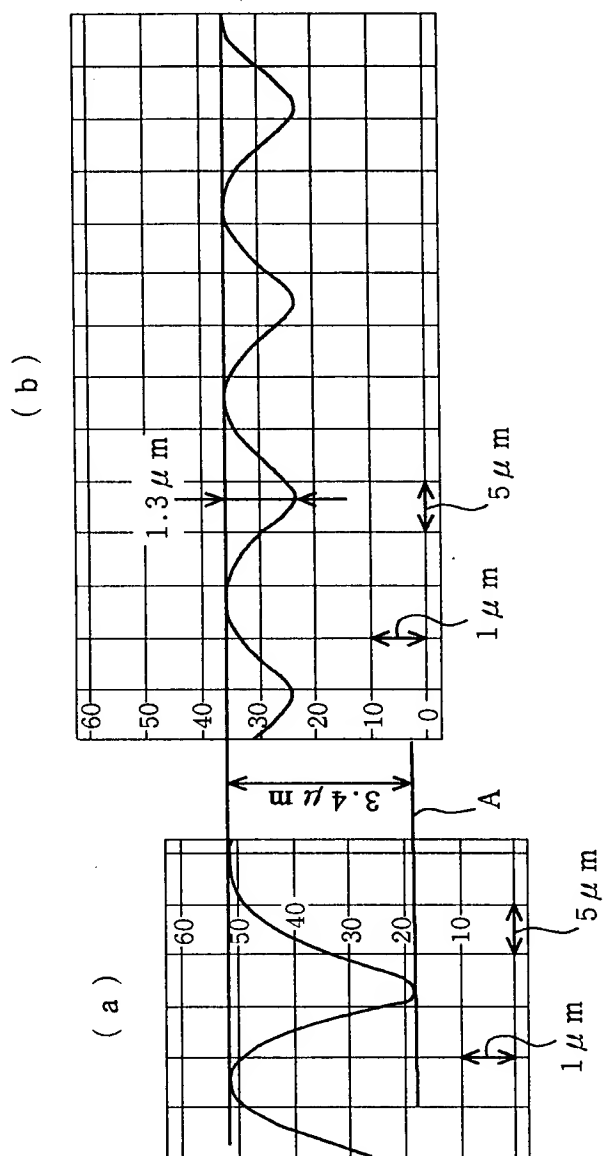


Fig 4

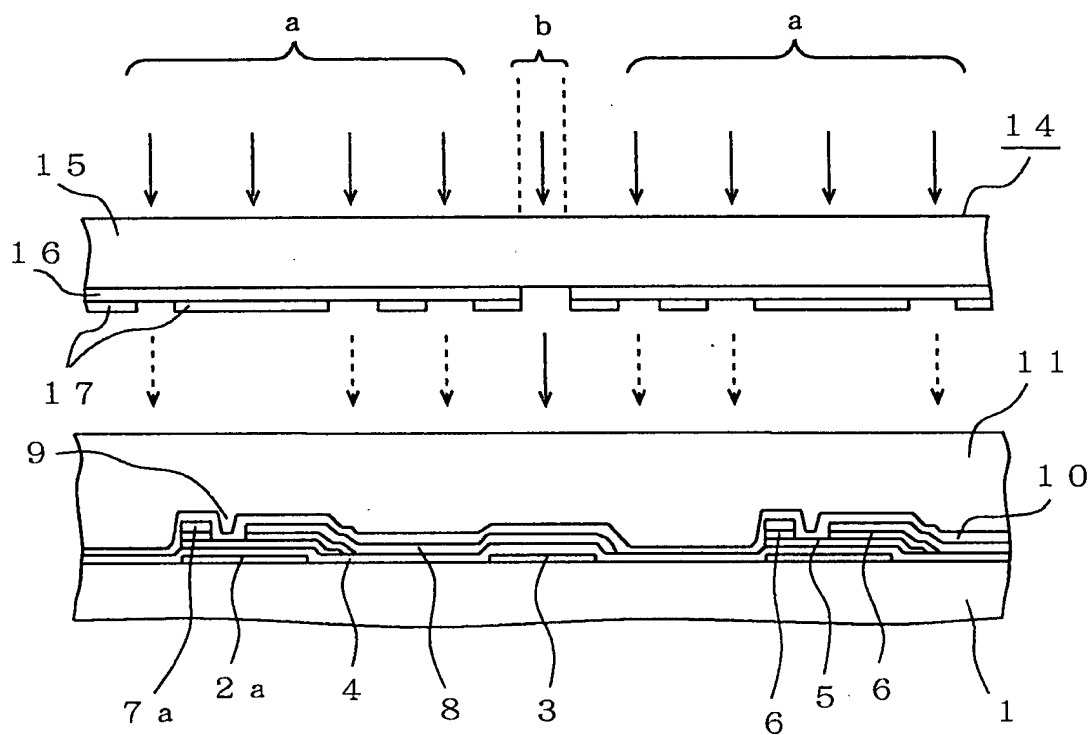


Fig 5

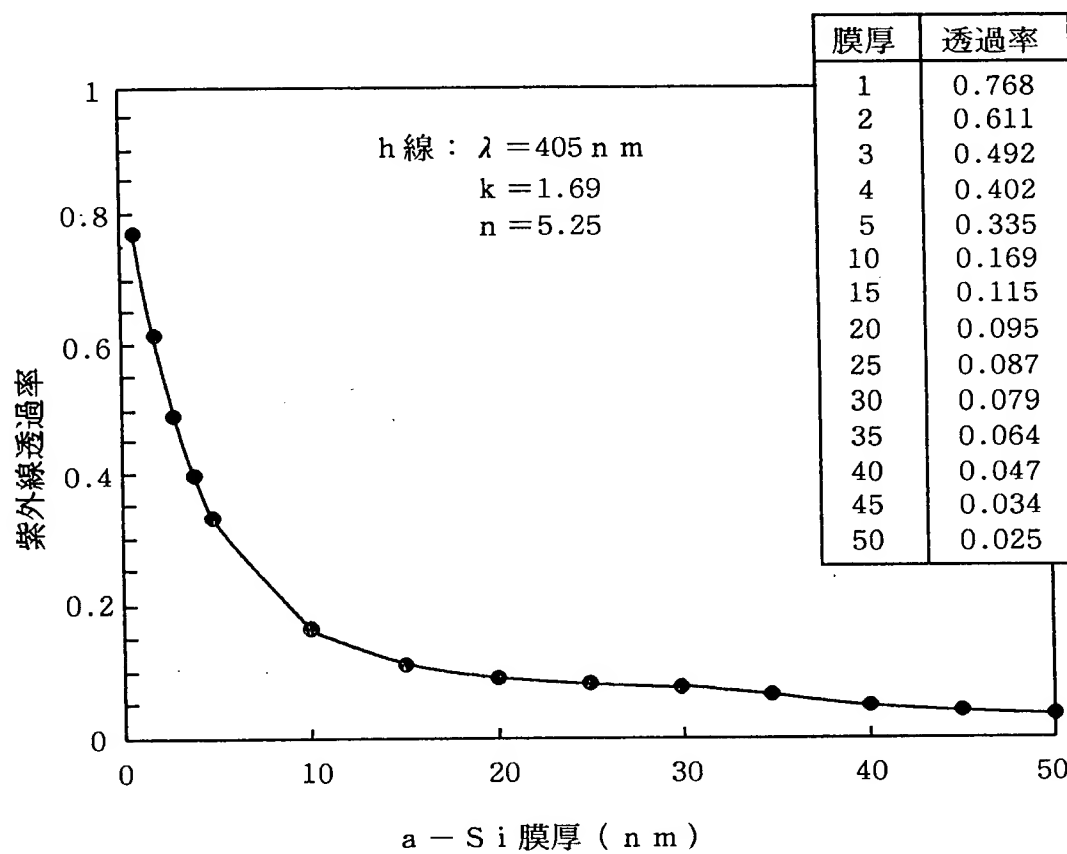


Fig 6

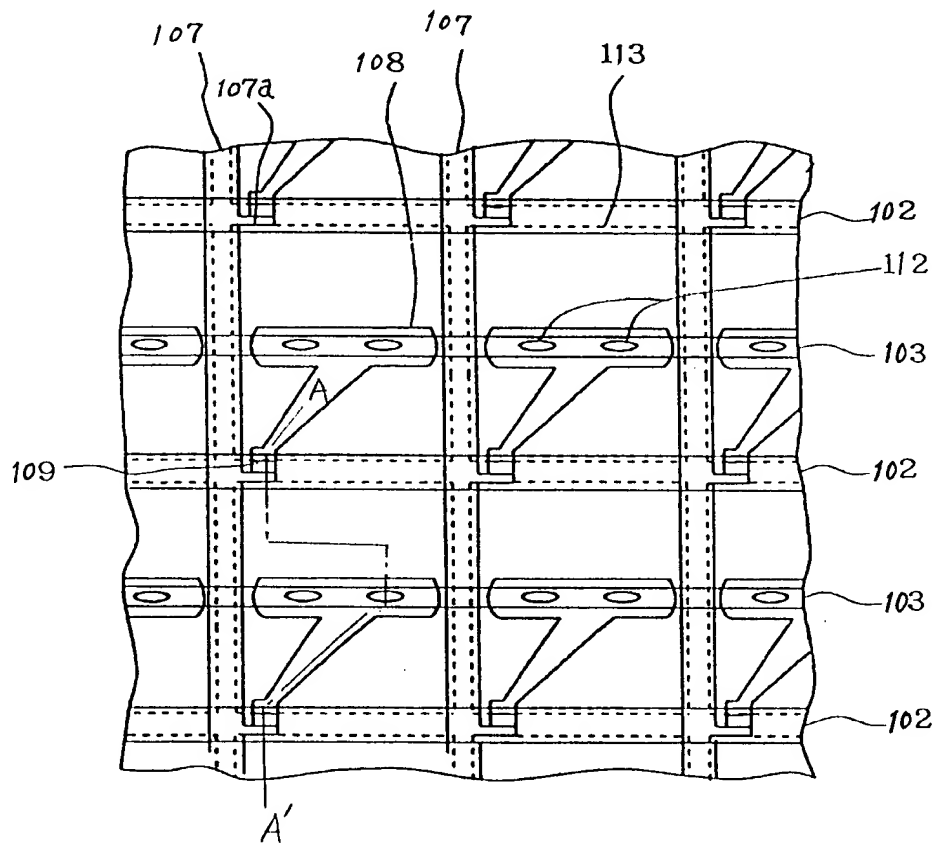
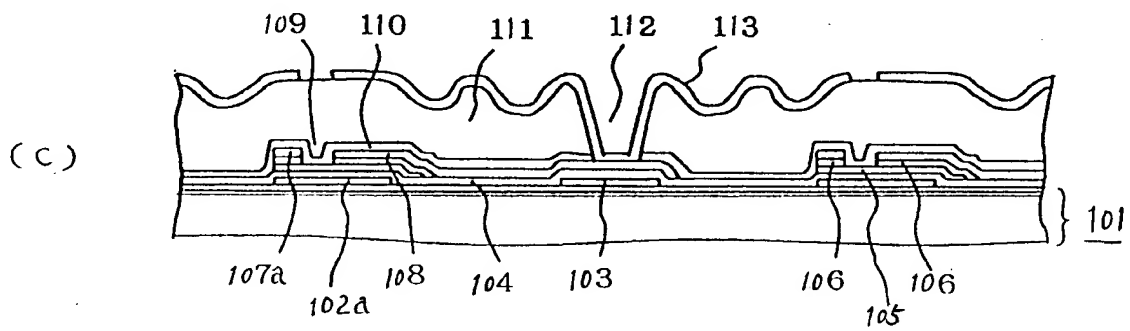
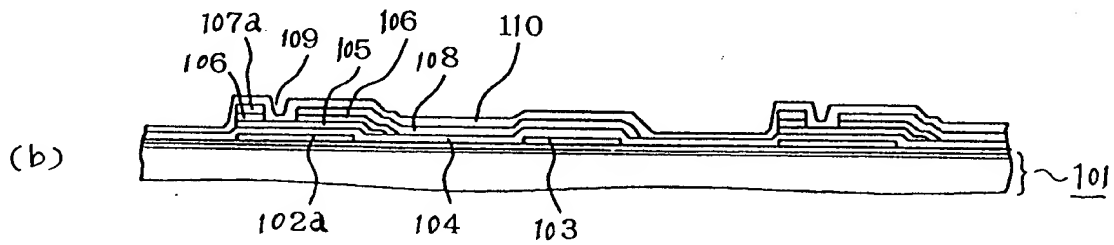
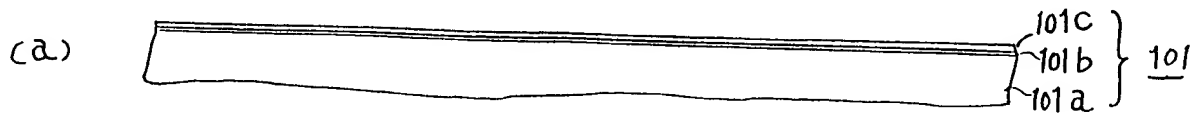
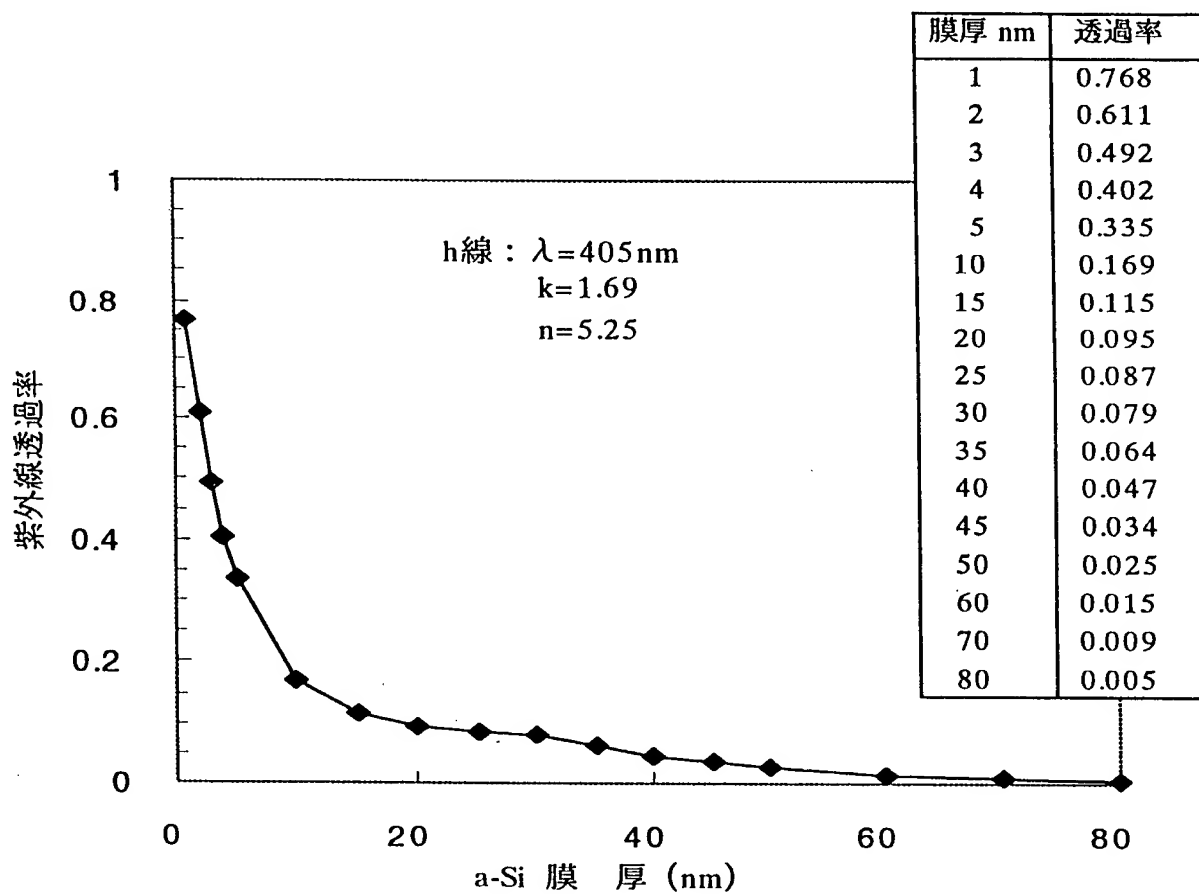


Fig 7



This figure is a schematic diagram of a substrate with a complex top layer structure. The substrate is labeled 101. The top layer is divided into several regions, each with a specific label. The regions are labeled 107a, 109, 106, 110, 108, 105, 102a, 104, and 103. The regions 107a, 109, 106, 110, 108, 105, 102a, 104, and 103 are shown in cross-section, with the substrate 101 at the bottom. The regions 107a, 109, 106, 110, 108, 105, 102a, 104, and 103 are shown in cross-section, with the substrate 101 at the bottom.

Fig 8



a-Si 膜厚に対する紫外線透過率 (計算値)

Fig 9

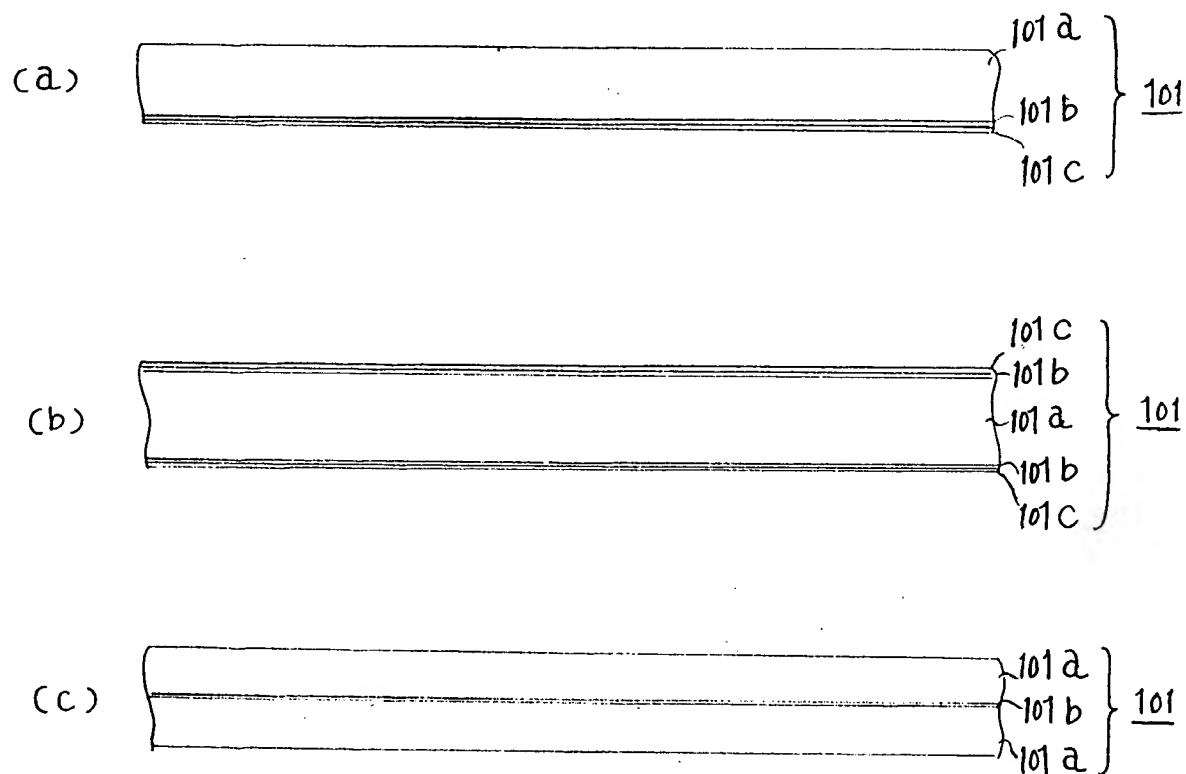


Fig 10

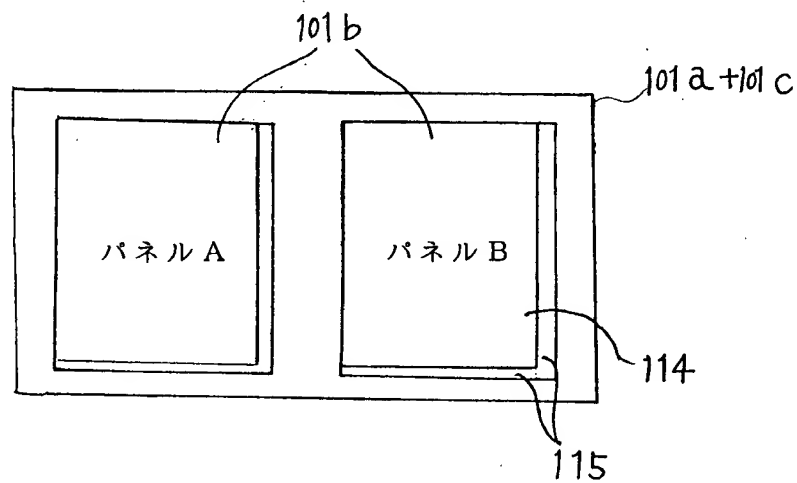


Fig 11

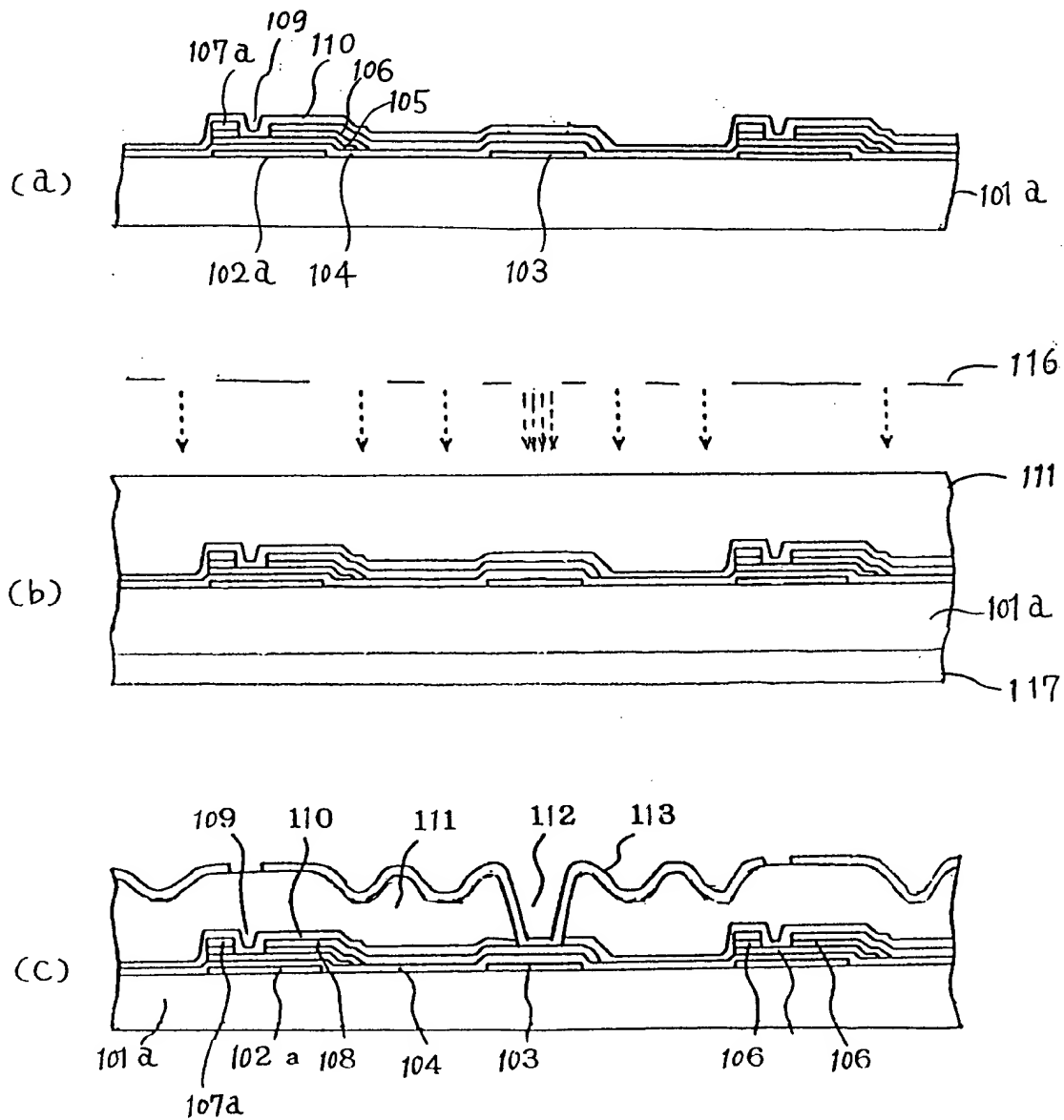


FIG. 11 is a cross-sectional view of a semiconductor device in a first embodiment. The device includes a substrate 101a, a layer 102a, a layer 104, a layer 103, and a layer 105. On top of these layers are several rectangular structures labeled 107a, 109, 110, and 106. The device is shown in a cross-sectional view.

Fig 12

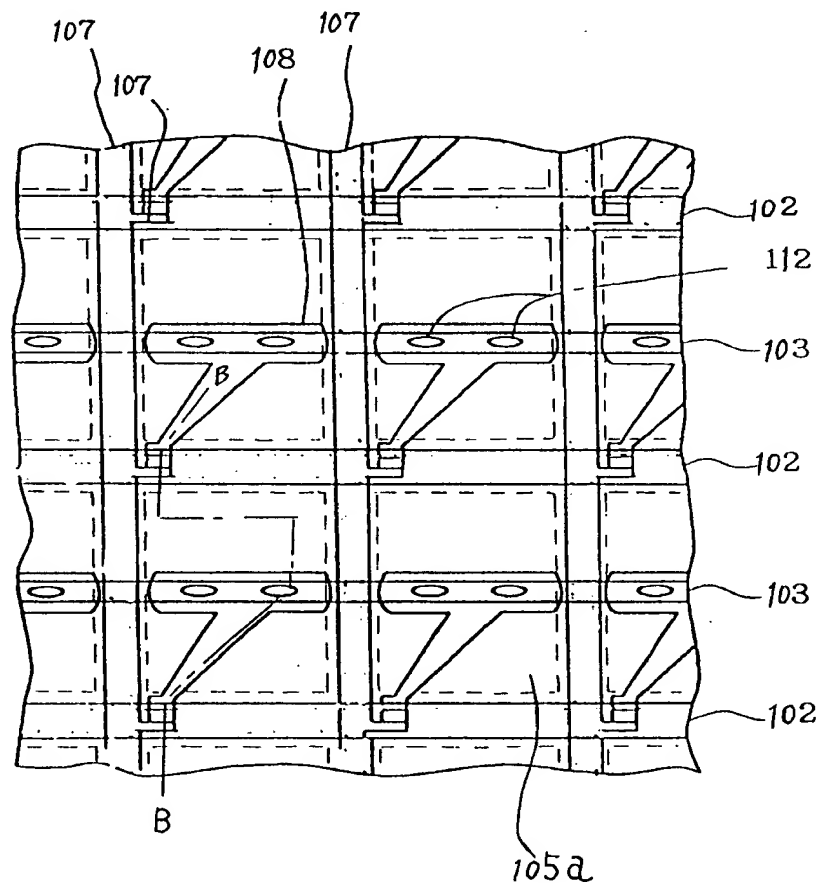


Fig 13

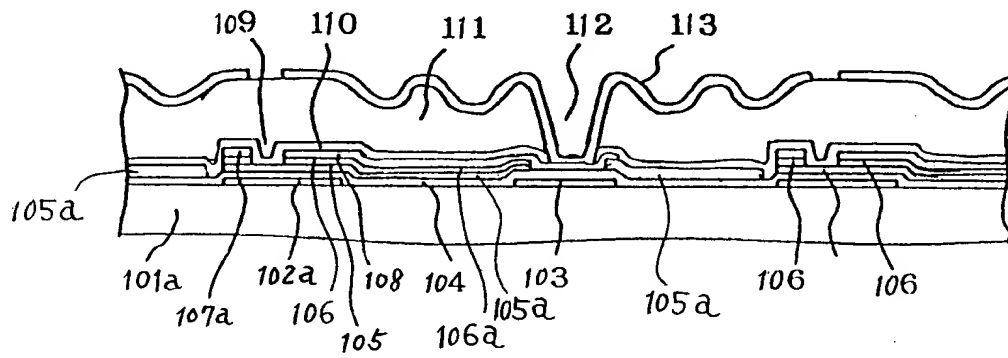


Fig 14

